12V MOSFET Drivers with Output Disable for Single Phase Synchronous-Rectified Buck Converter

General Description

The uP1959 is a dual, high voltage MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous-rectified buck converter. Each driver is capable of driving a 5000pF capacitive load with 30ns transition time. This device combined with uPI multi-phase buck PWM controller forms a complete core voltage regulator for advanced micro-processors.

The uP1959 features adaptive anti-shoot-through protection that prevents cross-conduction of the external MOSFET while maintains minimum deadtime for optimized efficiency.

This part has integrated bootstrap diode to help minimize the external component count. Both gate drives are turned off by pulling low OD# pin or high-impedance at PWM pin, preventing rapid output capacitor discharge during system shutdown.

This device also supports supply input under voltage lockout. The uP1959 is available in thermally enhanced WDFN2x2 - 8L and WDFN3x3 - 8L packages.

Ordering Information

Order Number	Package	Top Marking
uP1959PDN8	WDFN2x2 - 8L	DU
uP1959QDN8		EI
uP1959RDE8	WDFN3x3 - 8L	uP1959R

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

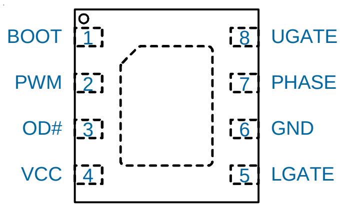
Features

- All-In-One Synchronous Buck Drivers
- Integrated Bootstrap Diode
- Adaptive Anti-Shoot-Through Protection Circuitry
- 1 PWM Signal Generates both Drivers
- Tri-State Input for Bridge Shutdown
- Output Disable Control Turans Off both MOSFETs
- Under Voltage Lockout for Supply Input
- WDFN2x2 - 8L and WDFN3x3 - 8L Packages
- RoHS Compliant and Halogen Free

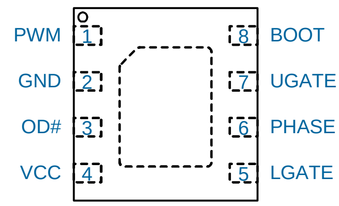
Applications

- Desktop CPU Core Voltage Regulators
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

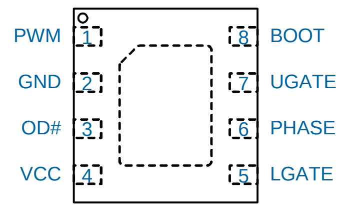
Pin Configuration



uP1959P

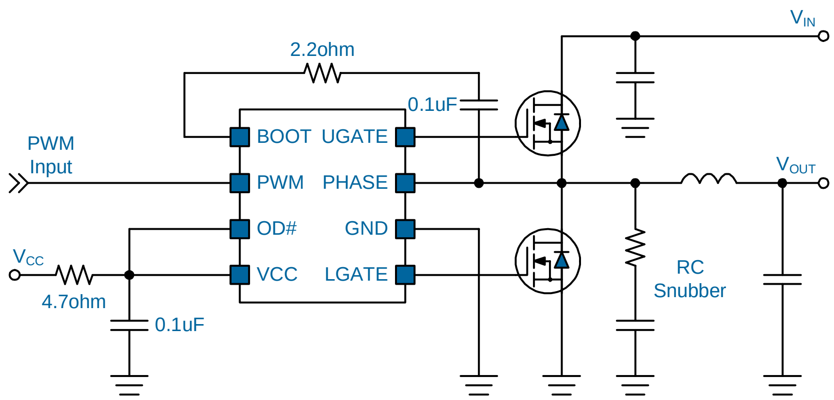


uP1959Q

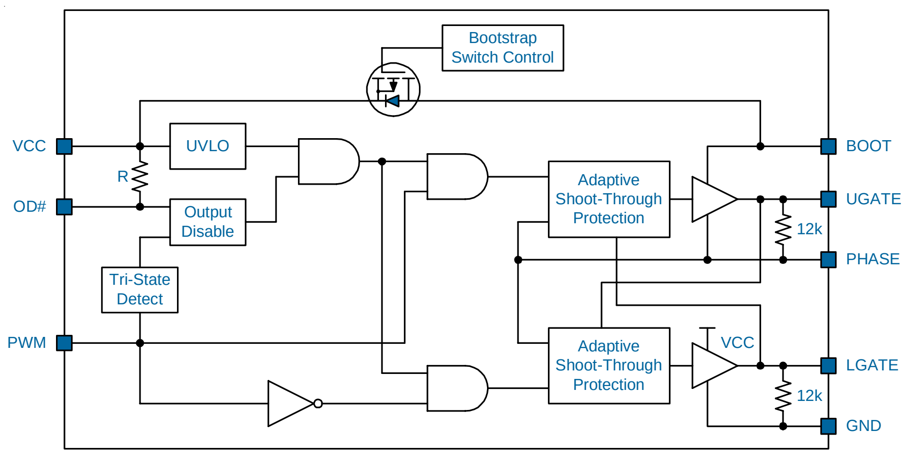


uP1959R

Typical Application Circuit



Functional Block Diagram



Functional Pin Description

Pin No.		Pin Name	Pin Function
PDN8	QDN8 /RDE8		
1	8	BOOT	**Bootstrap Supply** for the floating upper gate driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the PHASE pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Make sure that C_{BOOT} is placed near the IC.
2	1	PWM	**PWM Input.** This pin receives logic level input and controls the driver outputs.
3	3	OD#	**Output Disable.** This pin disables normal operation and forces both UGATE and LGATE off when it is pulled low. If this pin is left open, it is internally pulled high.
4	4	VCC	**Supply Voltage for the IC.** This pin provides bias voltage for the IC. Connect this pin to 12V voltage source and bypass it with an R/C filter.
5	5	LGATE	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has been turned off.
6	2	GND	**Ground for the IC.** All voltage levels are measured with respect to this pin.
7	6	PHASE	**PHASE Switch Node.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the return path for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has been turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
8	7	UGATE	**Upper Gate Driver Output.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has been turned off.
Exposed Pad			**Thermal Pad.** The exposed pad should be well soldered to PCB GND for effective heat conduction.

Functional Description

Output Disable

Logic low of OD# disables the gate drivers and keep both output low. Tie the OD# pin to controller power directly if the output disable function is not used.

PWM Input

The PWM pin is a tri-state input. Logic high turns on the high-side gate driver and turns off the low side gate driver once the POR of VCC is granted and OD# is kept high. Logic low turns off the high side gate driver and turns on the low side gate driver.

High impedance input at PWM pin will keep both high-side and low-side gate drivers low and turns off both MOSFETs. The PWM pin voltage is kept around 1.6V by internal bias circuit when floating.

Low-Side Driver

The low-side driver is designed to drive a ground-referenced N-channel MOSFET. The bias to the low-side driver is internally connected to VCC supply and GND. The low-side driver output is out of phase with the PWM input when it is enabled. The low side driver is held low if the OD# pin is pulled low or high-impedance at PWM pin.

High-Side Driver

The high-side driver is designed to drive a floating N-channel MOSFET. The bias voltage to the high-side driver is internally connected to BOOT and PHASE pins. An integrated bootstrap diode that is connected between BOOT and VCC pins provides the bias current for the high-side gate driver.

The bootstrap capacitor C_{BOOT} is charged to V_{CC} when PHASE pin is grounded by turning on the low-side MOSFET. The PHASE rises to V_{IN} when the high-side MOSFET is turned on, forcing the BOOT pin voltage to $V_{IN} + V_{CC}$ that provides voltage to hold the high-side MOSFET on.

The high-side gate driver output is in phase with the PWM input when it is enabled. The high-side driver is held low if the OD# pin is pulled low or high-impedance at PWM pin.

Adaptive Shoot Through Protection

The adaptive shoot-through circuit prevents the high-side and low-side MOSFETs from being turned on simultaneously and conducting destructive large current. It is done by turning on one MOSFET only after the other MOSFET is off already with adequate delay time.

At the high-side off edge, UGATE and PHASE voltages are monitored for anti-shoot-through protection. The low-side driver will not begin to output high until both (V_{UGATE} - V_{PHASE}) and V_{PHASE} are lower than 1.2V, making sure the high-side MOSFET is turned off completely.

At the low-side off edge, LGATE voltage is monitored for anti-shoot-through protection. The high-side driver will not begin to output high until V_{LGATE} is lower than 1.2V, making sure the low-side MOSFET is turned off completely.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC ---------- -0.3V to +15V
BOOT to PHASE ---------- -0.3V to +15V
PHASE to GND
DC ---------- -0.7V to 15V
< 200ns ---------- -8V to 30V
BOOT to GND
DC ---------- -0.3V to (VCC + 15V)
< 200ns ---------- -0.3V to 42V
UGATE to PHASE
DC ---------- -0.3V to (BOOT - PHASE +0.3V)
<200ns ---------- -5V to (BOOT - PHASE + 0.3V)
LGATE to GND
DC ---------- -0.3V to (VCC + 0.3V)
<200ns ---------- -5V to (VCC + 0.3V)
PWM ---------- -0.3V to +6V
OD# ---------- -0.3V to (VCC + 0.3V)
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
WDFN2x2 - 8L θ_{JA} ---------- 155°C/W
WDFN2x2 - 8L θ_{JC} ---------- 20°C/W
WDFN3x3 - 8L θ_{JA} ---------- 68°C/W
WDFN3x3 - 8L θ_{JC} ---------- 6°C/W
Power Dissipation, P_D @ T_A = 25°C
WDFN2x2 - 8L ---------- 0.65W
WDFN3x3 - 8L ---------- 1.47W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

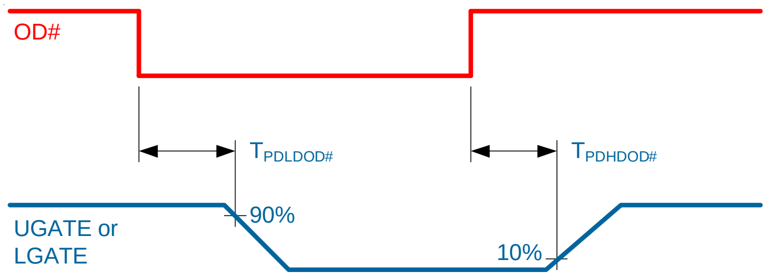
Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

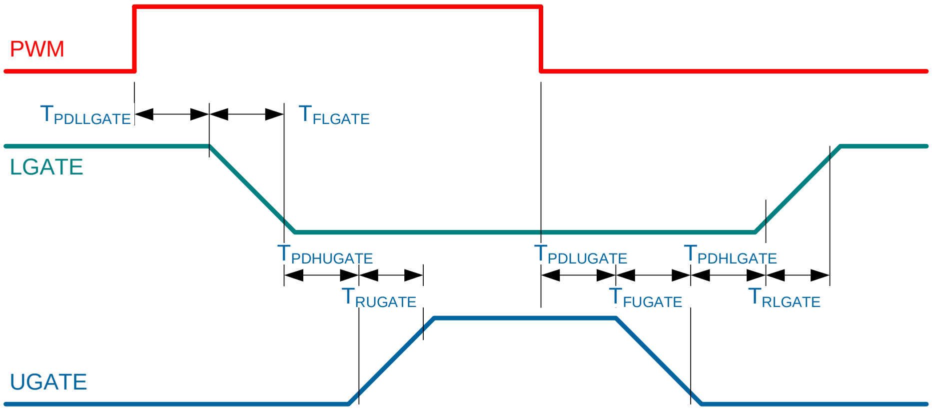
Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

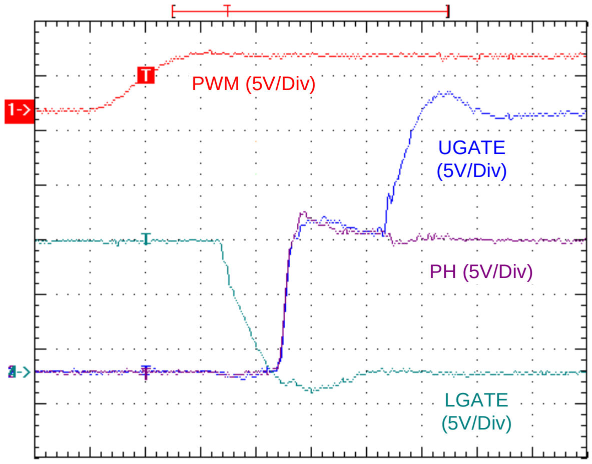
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Input Current	I_{CC}	PWM = OD# = 0V	--	1	2.5	mA
VCC POR Rising Threshold	V_{CCRTH}	V_{CC} rising	4.0	4.2	4.4	V
VCC POR Hysteresis	V_{CCHYS}		--	0.25	--	V
PWM Input						
Input High Threshold	PWM_{RTH}		2.3	2.5	2.7	V
Input Low Threshold	PWM_{FTH}		0.5	0.7	0.9	V
PWM Floating Voltage	PWM_{FLT}		--	1.6	--	V
PWM Input Current	I_{PWM}	PWM = 0V	-420	-280	-140	uA
		PWM = 3.3V	0.25	0.45	0.8	mA
		PWM = 5V	1.0	1.6	1.9	mA
Output Disable Input OD#						
Input High	$OD\#_H$		2.0	--	--	V
Input Low	$OD\#_L$		--	--	0.6	V
OD# Pin Pull-High Current	$I_{OD\#\_SRC}$		--	10	--	uA
Propagation Delay Time	$T_{PDHDOD\#}$		--	20	45	ns
	$T_{PDLDOD\#}$		--	300	--	ns
Bootstrap Switch						
On Resistance	$R_{DS(ON)}$	Forward bias current = 1mA	--	40	--	Ω
High Side Driver						
Output Resistance, Sourcing	R_{H_SRC}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = -80mA	--	1.2	2.4	Ω
Output Resistance, Sinking	R_{H_SNK}	V_{BOOT} - V_{PHASE} = 12V, I_{UGATE} = 80mA	--	0.8	1.6	Ω
Output Rising Time	T_{RUGATE}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T_{FUGATE}	V_{BOOT} - V_{PHASE} = 12V, C_{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	$T_{PDHUGATE}$	V_{BOOT} - V_{PHASE} = 12V	--	40	65	ns
	$T_{PDLUGATE}$	V_{BOOT} - V_{PHASE} = 12V	--	20	35	ns
Low Side Driver						
Output Resistance, Sourcing	R_{L_SRC}	V_{CC} = 12V, I_{LGATE} = -80mA	--	1.2	2.4	Ω
Output Resistance, Sinking	R_{L_SNK}	V_{CC} = 12V, I_{LGATE} = 80mA	--	0.8	1.6	Ω
Output Rising Time	T_{RLGATE}	V_{CC} = 12V, C_{LOAD} = 3nF	--	35	45	ns
Output Falling Time	T_{FLGATE}	V_{CC} = 12V, C_{LOAD} = 3nF	--	20	30	ns
Propagation Delay Time	$T_{PDHLGATE}$	V_{CC} = 12V	--	40	65	ns
	$T_{PDLLGATE}$	V_{CC} = 12V	--	20	35	ns


OD#
$T_{PDLDOD\#}$
$T_{PDHDOD\#}$
UGATE or LGATE
90%
10%


PWM
$T_{PDLLGATE}$
T_{FLGATE}
LGATE
$T_{PDHUGATE}$
T_{RUGATE}
$T_{PDLUGATE}$
T_{FUGATE}
$T_{PDHLGATE}$
T_{RLGATE}
UGATE

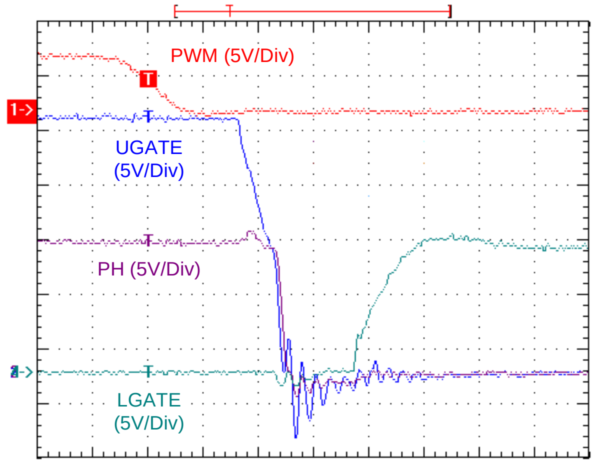
Typical Operation Characteristics

LG Falling to UG Rising Dead Time



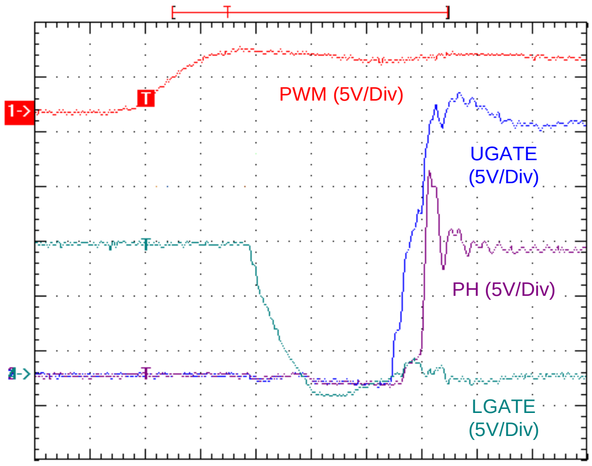
20ns/Div
V_{IN} = 12V, VCC = 12V, HSFET = QM3004*1,
LSFET = QM3006*2, Converter Load = 0A

UG Falling to LG Rising Dead Time



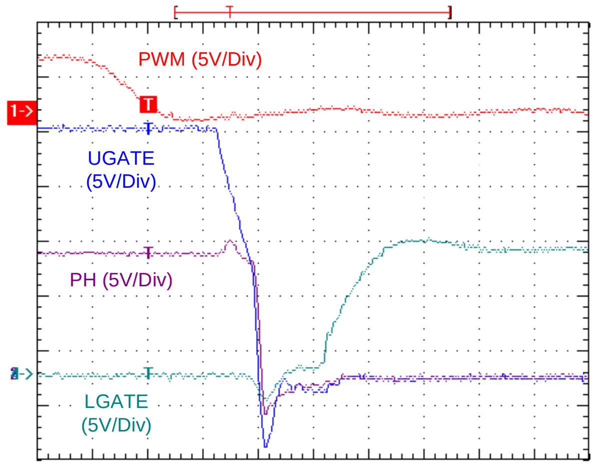
20ns/Div
V_{IN} = 12V, VCC = 12V, HSFET = QM3004*1,
LSFET = QM3006*2, Converter Load = 0A

LG Falling to UG Rising Dead Time



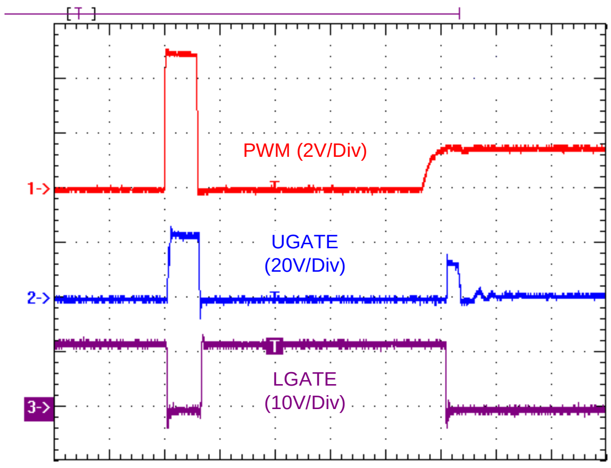
20ns/Div
V_{IN} = 12V, VCC = 12V, HSFET = QM3004*1,
LSFET = QM3006*2, Converter Load = 15A

UG Falling to LG Rising Dead Time



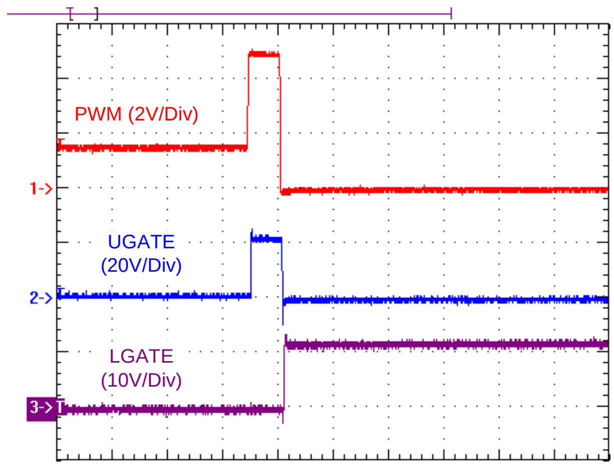
20ns/Div
V_{IN} = 12V, VCC = 12V, HSFET = QM3004*1,
LSFET = QM3006*2, Converter Load = 15A

PWM Enter Tristate Operation



1us/Div
V_{IN} = 12V, VCC = 12V, HSFET = QM3004*1,
LSFET = QM3006*2, Converter Load = 0A

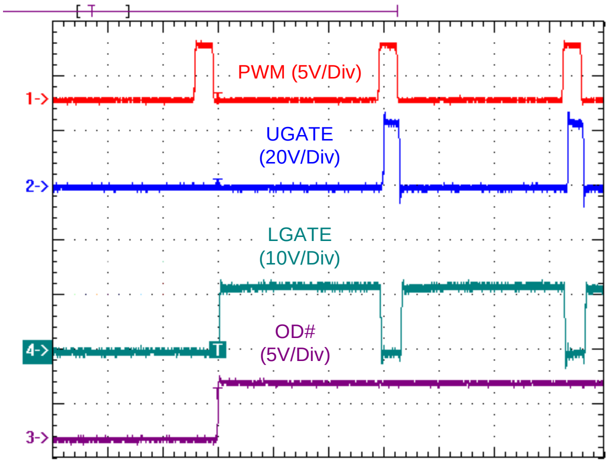
PWM Exit Tristate Operation



1us/Div
V_{IN} = 12V, VCC = 12V, HSFET = QM3004*1,
LSFET = QM3006*2, Converter Load = 0A

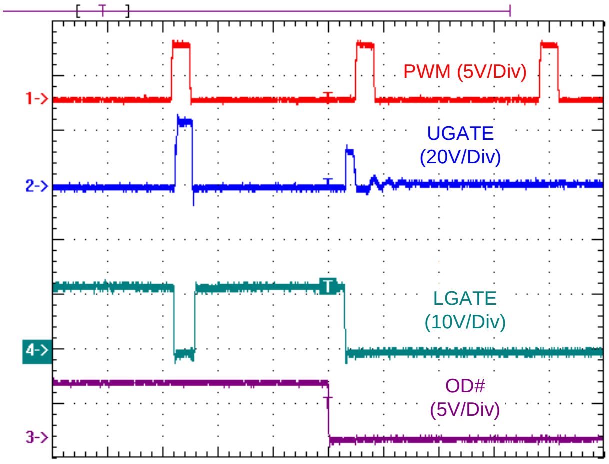
Typical Operation Characteristics

OD# Rising Propagation Delay Time



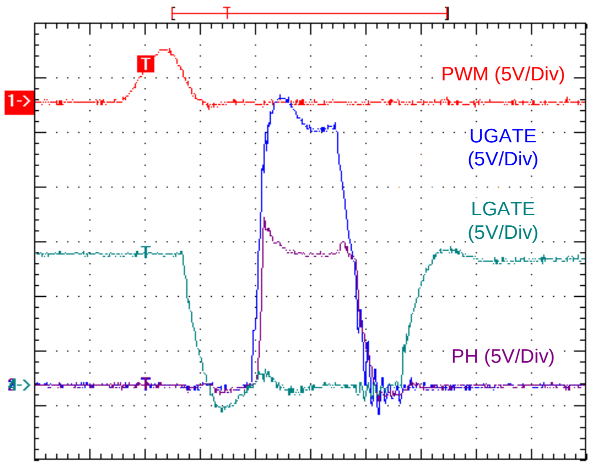
1us/Div
V_{IN} = 12V, VCC = 12V

OD# Falling Propagation Delay Time



1us/Div
V_{IN} = 12V, VCC = 12V

Short Pulse



40ns/Div
V_{IN} = 12V, VCC = 12V

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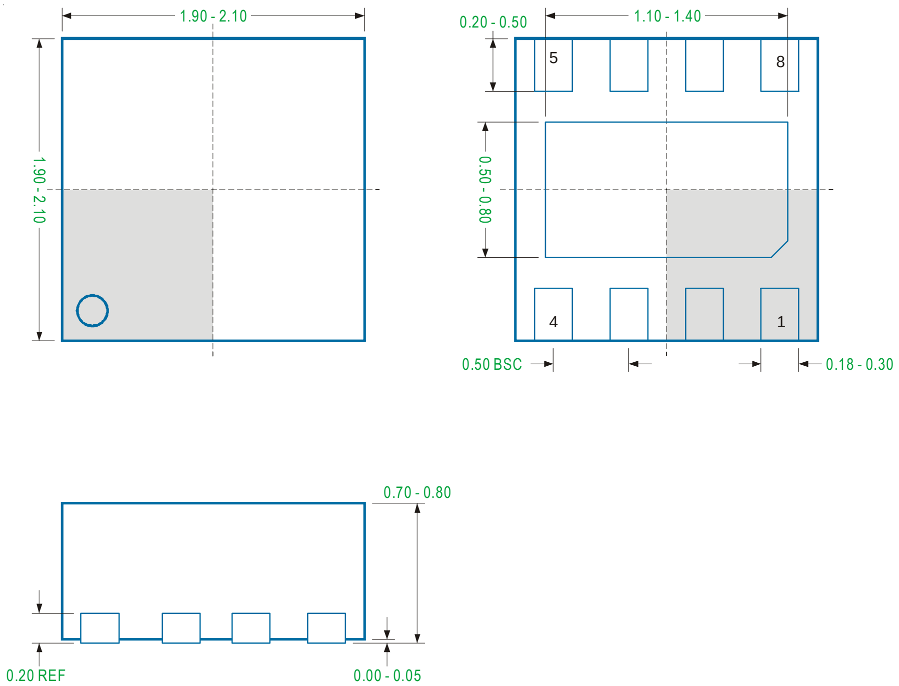
Package Information

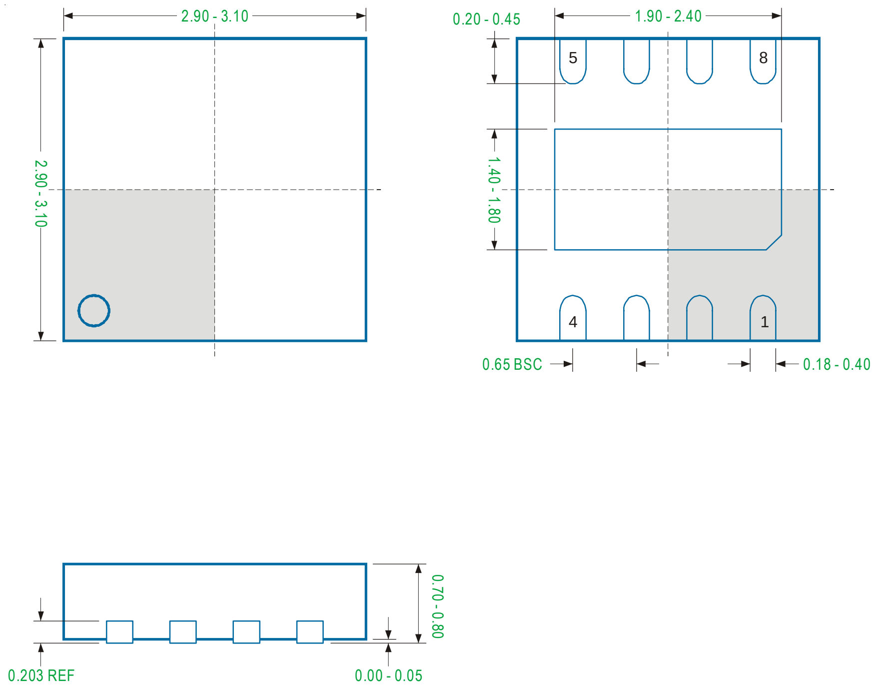
WDFN2x2 - 8L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

WDFN3x3 - 8L



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   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

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